UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,300	11/24/2003	Kenway W. Tam	SUNMP351	7065

32291 7590 03/22/2006

MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,300	TAM ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181
3/17/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Elements 120A, 120B, 122A, 122B, 124A, 124B, 126, 126A, and 126B of figure 1B; elements 120A, 120B, 222A, 222B, 224A, and 224B of figure 2A; 310A, 310B, 310C, 312A, 312B, 312C, 314A, 314B, 314C, 316A, 316B, and 316C of figure 3. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: On page 2 of the specification, the phrase "can be can be" is used in paragraph 4, line 10. It is suggested to be changed to "can be."

Appropriate correction is required.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Internal Pipeline Architecture for Save/Restore Operations on Register Swaps to Reduce Latency.

Claim Objections

4. Claim 6 objected to because of the following informalities:

As per claim 6, the term "delayed sufficient to allow" is a grammatically mistake. It is suggested to and assumed to read "delayed sufficiently to allow." An alternative is "delayed sufficient time to allow."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear as to what is meant by "the same register further includes the same register in a same processing thread." For the purpose of examination, it is assumed to refer to an instruction in a thread containing reference to a register.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-3 and 9-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. There are no tangible end results from implementing the claims in question because the end result is a determination, which lacks a tangible "real world" result. Although some claims do have intermediate steps that produce an intermediate tangible result, the end result is merely a determination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being unpatentable over Hennessy et al (Computer Architecture: A Quantitative Approach), herein referred to as Hennessy et al.

As per claim 1, Hennessy et al discloses a method for processing a plurality of swap requests (See sections 3.3-3.4: Hennessy et al teaches situation where data hazards may come from and ways to handle those hazards) comprising:

receiving a first swap request in a pipeline (See section 3.3. figure 3.5, page 142 and section 2.8, figure 2.25, page 104: The first swap is Instruction 1 and the various move instructions, such as MOVI2S, MOVS2I, etc, are instructions for swapping);

executing the first swap request (See section 3.3. figure 3.5, page 142 and section 2.8, figure 2.25, page 104: The DLX pipeline can handle instructions such as moves);

receiving a second swap request in the pipeline immediately subsequent to the first swap request (See section 3.3. figure 3.5, page 142: and section 2.8, figure 2.25, page 104: The second swap is Instruction 2 and the various move instructions, such as MOVI2S, MOVS2I, etc, are instructions for swapping); and

determining if the first swap request and the second swap request swap a same register (See sections 3.3-3.4: Determining if the first swap request and the second

swap request swap a same register is part of the hazard detection that must go on in order to properly prevent hazards in the pipeline).

As per claim 2, Hennessy et al discloses further comprising executing the second swap request if the first swap request and the second swap request do not swap the same register (See section 3.3, figure 3.6, page 142: It would be as if the first swap is Instruction 1 and the second swap is Instruction 2, whereas no conflicts/hazards arise).

As per claim 3, Hennessy et al discloses wherein the first swap request includes a first save operation and a first restore operation and the second swap request includes a second save operation and a second restore operation (See section 2.8, figure 2.25, page 104: These steps of operation are embodied in the various move instructions).

As per claim 4, Hennessy et al discloses wherein executing the second swap request if the first swap request and the second swap request do not swap the same register includes executing the first restore operation and the second save operation substantially simultaneously (See section 3.4, figure 3.12, page 153: With data forwarding a register can be written to and read at the same time).

As per claim 5, Hennessy et al discloses further comprising: delaying execution of the second swap request if the first swap request and the second swap request swap

the same register (See section 3.3, figure 3.7, page 143: The delaying of an execution is represented by the stall); and executing the second swap request (See section 3.3, figure 3.7, page 143: The instruction starts execution after the stall).

As per claim 6, Hennessy et al discloses wherein the execution of the second swap request is delayed sufficient to allow the execution of the first swap request to be completed (See section 3.3, figure 3.7, page 139 and 143 and page: Stalling is done as long as it is necessary to ensure proper execution of instructions).

As per claim 7, Hennessy et al discloses wherein the execution of the second swap request is delayed a predetermined number of clock cycles (See section 3.3, figure 3.6, page 142, and figure 3.7, page 143: Lengths of stalls are based on number of clock cycles and on a basic 5 stage pipeline, as shown in the DLX model, a stall can take up as much as 3 cycles. The type of stall determines the length of a stall).

As per claim 8, Hennessy et al discloses wherein the execution of the second swap request is delayed one clock cycle (See section 3.4, figure 3.13, page 154 and pages 152-155; The figure shows where with data forwarding a stall can be limited to just one clock cycle and doing multiple moves is a case where data hazards require stalls since the pipeline must wait until the data is about to be written to a register before it can be forwarded to the next instruction).

As per claim 9, Hennessy et al discloses wherein the pipeline includes more than one processing thread (See section 3.7, pages 187-199: The basic DLX pipeline is extended to include multiple stages of execution (as shown in figure 3.44 on page 190) meaning that instructions are split up among the different execution stages. Those groups of split up instructions are known as threads).

As per claim 10, Hennessy et al discloses wherein the same register further includes the same register in a same processing thread (See section 3.7, pages 187-199: An instruction in a thread will include a register).

As per claim 11, Hennessy et al discloses wherein determining if the first swap request and the second swap request swap the same register occurs as the second swap request is received (See section 3.4, figure 3.13, page 154: The stall bubble does not occur until instruction is received an decoded).

As per claim 12, Hennessy et al discloses a method for processing a plurality of consecutive swap requests (See sections 3.3-3.4: Hennessy et al teaches situation where data hazards may come from and ways to handle those hazards) in a multithreaded microprocessor pipeline (See section 3.7, pages 187-199: The basic DLX pipeline is extended to include multiple stages of execution (as shown in figure 3.44 on page 190), meaning that instructions are split up among the different execution stages. Those groups of split up instructions are known as threads) comprising:

receiving a first swap request in a pipeline (See section 3.3. figure 3.5, page 142 and section 2.8, figure 2.25, page 104: The first swap is Instruction 1 and the various move instructions, such as MOVI2S, MOVS2I, etc, are instructions for swapping);

executing the first swap request (See section 3.3. figure 3.5, page 142 and section 2.8, figure 2.25, page 104: The DLX pipeline can handle instructions such as moves);

receiving a second swap request in the pipeline (See section 3.3. figure 3.5, page 142: and section 2.8, figure 2.25, page 104: The second swap is Instruction 2 and the various move instructions, such as MOVI2S, MOVS2I, etc, are instructions for swapping); and

determining if the first swap request and the second swap request swap a same register in a same processing thread (See sections 3.3-3.4: Determining if the first swap request and the second swap request swap a same register is part of the hazard detection that must go on in order to properly prevent hazards in the pipeline).

As per claim 13, Hennessy et al discloses further comprising executing the second swap request if the first swap request and the second swap request do not swap the same register (See section 3.3, figure 3.6, page 142: It would be as if the first swap is Instruction 1 and the second swap is Instruction 2, whereas no conflicts/hazards arise).

As per claim 14, Hennessy et al discloses further comprising: delaying execution of the second swap request at least one clock cycle if the first swap request and the second swap request swap the same register (See section 3.3, figure 3.7, page 143: The delaying of an execution is represented by the stall); and executing the second swap request (See section 3.3, figure 3.7, page 143: The instruction starts execution after the stall).

As per claim 15, Hennessy et al discloses a plurality of pipeline registers (See section 2.8, page 98: There are 32 registers), at least one of the plurality of pipeline registers being capable of comparing a first swap request and a second swap request (See sections 3.3-3.4: Determining if the first swap request and the second swap request swap a same register is part of the hazard detection that must go on in order to properly prevent hazards in the pipeline and any register is capable of doing a move); and a plurality of active registers (See section 2.8, page 98: The floating point registers can be used as active registers).

As per claim 16, Hennessy et al discloses wherein the plurality of pipeline registers includes at least eight pipeline registers, and wherein the at least eight pipeline registers are linked to one of the plurality of active registers (See section 2.8, page 98: There are 32 general purpose registers and a plurality of floating point registers which can be used as pipeline registers and active registers, respectively).

As per claim 17, Hennessy et al discloses wherein the plurality of pipeline registers includes 32 pipeline registers (See section 2.8, page 98: There are 32 general purpose registers).

As per claim 18, Hennessy et al discloses wherein the pipeline architecture is one of at least two pipeline architectures in a single multithreaded microprocessor (See section 3.7, figure 3.44, page 190: The basic DLX pipeline is extended to include multiple stages of execution).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show art related to internal pipeline architecture for save/restore operations on register swaps to reduce latency:

U.S. Patent # 4,831,623 to Terzian shows swap scan testing of digital logic.

U.S. Patent # 5,634,118 to Blomgen shows splitting a floating-point stack exchange instruction for merging into surrounding instructions by operand translation through the use of swap instructions.

U.S. Patent # 5,819,060 to Cesana shows an instruction swapping in a dual pipeline microprocessor.

U.S. Patent # 6,549,442 B1 to Lu et al shows hardware-assisted fast bank-swap in a content-addressable-memory processor

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

AU 2181 3/17/2006

vl
March 15, 2006